

**IN THE CLAIMS**

Please amend the claims as follows:

1. (Cancelled)
2. (Currently amended) ~~[[The]]~~ A packet transmission/reception processor coupled to a CPU, the processor of Claim 1, further comprising:  
a link core circuit for receiving a packet externally delivered through a bus;  
a packet processing controller for processing the packet received by the link core circuit,  
generating a packet to be transmitted in response to the received packet, and supplying the packet to  
be transmitted to the link core circuit; and  
  
a packet processing control timer for clocking how much time has passed since the packet was received by the link core circuit and for generating a signal when the time passed reaches a predetermined amount of time,  
  
wherein the link core circuit sends out the packet to be transmitted, supplied from the packet processing controller, by way of the bus, and  
  
responsive to the signal supplied from the packet processing control timer, the packet processing controller stops processing the received packet, generates ~~makes~~ another packet to be transmitted in response to the received packet and ~~then~~ restarts processing the received packet.
3. (Currently amended) The processor of Claim ~~[[1]]~~ 2, wherein while processing the received packet, the controller prohibits the link core circuit from receiving another packet delivered externally through the bus.
4. (Currently amended) The processor of Claim ~~[[1]]~~ 2, further comprising a packet filter circuit for determining, by identification information included in each of the packets received by

the link core circuit, whether or not each said received packet should be processed and for supplying only the received packets to be processed to the controller.

5. (Original) The processor of Claim 4, wherein in accordance with the identification information of each said received packet and based on a result of the processing that the controller has performed on the received packet,

the filter circuit predicts header information of a packet that the link core circuit should receive next time; compares the predicted header information to header information of a next packet that the link core circuit has actually received; determines, based on a result of the comparison, whether or not the next packet received by the link core circuit should be stored; and then supplies only the packets to be stored to the controller.

6. (Currently amended) The processor of Claim ~~[[1]]~~ 2, wherein the controller comprises:  
a transaction control circuit for controlling a series of transactions, each starting with packet transmission and ending with packet reception or vice versa;

a packet engine circuit for automatically dividing a packet and controlling all the transactions;

a header control circuit for making a packet that includes a header with packet identification information but no data field and for controlling transmission of the packet;

a data field control circuit for making a packet that includes not only a header with packet identification information but also a data field and for controlling transmission of the packet; and

a data processing circuit for processing and controlling the data field of the received packets.

7. (Original) The processor of Claim 6, wherein the transaction control circuit manages a time it takes to transmit a packet after the controller started to make the packet or to finish processing a received packet after the controller received the packet, outputs a result of the time

management to the CPU and also manages a time it takes for the CPU to transmit a packet after the CPU started to make the packet or to finish processing a received packet after the CPU received the packet.

8. (Currently amended) A packet transmission/reception processor coupled to a CPU, the processor comprising:

a packet processing controller for making a packet to be transmitted; [[and]]

a link core circuit for sending out the packet to be transmitted, which has been made by the controller, to an external unit by way of a bus; and ~~for receiving a packet delivered externally through the bus,~~

a packet processing control timer for clocking how much time has passed since the packet processing controller starts to generate the packet to be transmitted and for generating a signal when the packet to be transmitted is not sent out after the time passed reaches a predetermined amount of time,

wherein the packet processing controller processes the packet received by the link core circuit, and makes a stops generating the packet to be transmitted in response to the ~~received packet~~ signal supplied from the packet processing control timer and ~~supplies the restarts generating the~~ packet to be transmitted ~~to the link core circuit after having processed the received packet~~ when a transaction processing performed by the CPU is completed.

9-10. (Canceled)

11. (New) The processor of Claim 8, wherein the controller comprises:

a transaction control circuit for controlling a series of transactions, each starting with packet transmission and ending with packet reception or vice versa;

a packet engine circuit for automatically dividing a packet and controlling all the transactions;

a header control circuit for making a packet that includes a header with packet identification information but no data field and for controlling transmission of the packet;

a data field control circuit for making a packet that includes not only a header with packet identification information but also a data field and for controlling transmission of the packet; and

a data processing circuit for processing and controlling the data field of the received packets.

12. (New) The processor of Claim 11, wherein the transaction control circuit manages a time it takes to transmit a packet after the controller started to generate the packet or to finish processing a received packet after the controller received the packet, outputs a result of the time management to the CPU and also manages a time it takes for the CPU to transmit a packet after the CPU started to generate the packet or to finish processing a received packet after the CPU received the packet.

13. (New) A packet transmission/reception processor coupled to a CPU, the processor comprising:

a link core circuit for receiving a packet externally delivered through a bus; and

a packet processing controller for processing the packet received by the link core circuit, generating a packet to be transmitted in response to the received packet, and supplying the packet to be transmitted to the link core circuit,

wherein the link core circuit sends out the packet to be transmitted, supplied from the packet processing controller, by way of the bus, and

while processing the received packet, the controller prohibits the link core circuit from receiving another packet delivered externally through the bus.

14. (New) The processor of Claim 13, further comprising a packet filter circuit for determining, by identification information included in each of the packets received by the link core circuit, whether or not each said received packet should be processed and for supplying only the received packets to be processed to the controller.

15. (New) The processor of Claim 14, wherein in accordance with the identification information of each said received packet and based on a result of the processing that the controller has performed on the received packet,

the filter circuit predicts header information of a packet that the link core circuit should receive next time; compares the predicted header information to header information of a next packet that the link core circuit has actually received; determines, based on a result of the comparison, whether or not the next packet received by the link core circuit should be stored; and then supplies only the packets to be stored to the controller.

16. (New) The processor of Claim 13, wherein the controller comprises:

a transaction control circuit for controlling a series of transactions, each starting with packet transmission and ending with packet reception or vice versa;

a packet engine circuit for automatically dividing a packet and controlling all the transactions;

a header control circuit for making a packet that includes a header with packet identification information but no data field and for controlling transmission of the packet;

a data field control circuit for making a packet that includes not only a header with packet identification information but also a data field and for controlling transmission of the packet; and

a data processing circuit for processing and controlling the data field of the received packets.

17. (New) The processor of Claim 16, wherein the transaction control circuit manages a time it takes to transmit a packet after the controller started to generate the packet or to finish processing a received packet after the controller received the packet, outputs a result of the time management to the CPU and also manages a time it takes for the CPU to transmit a packet after the CPU started to generate the packet or to finish processing a received packet after the CPU received the packet.